

A Novel Readout Circuit for On-sensor Multispectral Classification

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Abstract— A new readout integrated circuit (ROIC) for multispectral classification is presented. The ROIC is designed to utilize the spectral response tunability of dot-in-a-well (DWELL) infrared photodetector to exploit the possibility of real-time on-chip multispectral imaging for classification in analog domain. The unit cells are designed to include all necessary elements needed for spectral classification, including high-voltage time-varying positive and negative biases, bipolar integration, and selective sample-and-hold circuits. A test chip was designed and fabricated using TSMC's 0.35 μm high-voltage technology. The test chip has successfully completed its initial functional tests and is ready for hybridization to a DWELL focal-plane array.

Keywords— Readout integrated circuit, ROIC, CMOS image sensors, and multispectral classification, smart pixel

I. INTRODUCTION

Multispectral imaging and classification is an important task that is normally performed by utilizing a broadband detector with a set of narrowband filters that are physically placed in front of the broadband detectors. The mechanical parts required holding and switching the filters, and the cost associated with such a filters are a limiting factor for this approach [1].

To circumvent these drawbacks, our group presented a novel algorithm to perform multispectral imaging and classification by the utilization of the continuous bias tunability of the dot-in-well (DWELL) infrared photodetector [2], [3].

Figure 1.a shows an example of the grown structure of a single DWELL photodetector and Figure 1.b shows the impact of changing the applied bias voltage on the spectral response of the DWELL detector. Nonetheless, the spectral response of the DWELL photodetector at each bias voltage is 1-2 μm broad and has significant overlap with the spectral response associated with other bias voltages [3]. The spectral-tuning algorithm reported in [2] aimed to address the spectral overlap by forming a weighted superposition of photocurrents, obtained from using different biases, that optimally estimates (in the least-square sense) the ideal narrow-band photocurrent that would be obtained if we were to use a broadband detector to probe the same target of interest through a physical spectral filter having the desired narrow band. Moreover, our group developed a refinement of the algorithm that identifies a minimal set of only four biases to enable sensing only the relevant spectral information for specific remote-sensing applications of interest [4].

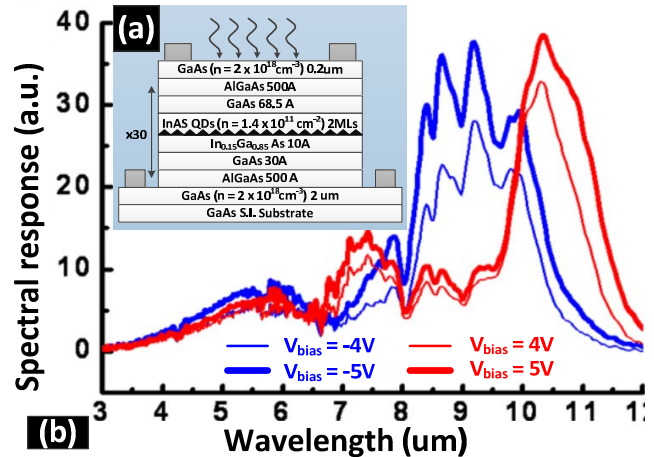


Fig. 1. a) Bias-voltage-dependent spectral responses of a DWELL photodetector showing potential for multispectral sensing. b) Grown structure of the DWELL photodetector. Pictures adopted from [2]

For the purpose of this paper, the application of interest is the classification of three types of rocks: granite, hornfels and limestone. From our previous results [4], we know that these rocks can be correctly classified by computing the synthesized feature vector, which is the linear combination of the incoming test photocurrent with the optimal pre-computed set of weights (one for each rock type). Since the set of weights are optimally matched to the spectra of each rock type, the feature component with the maximum value is the assigned class [4]. Based on our previous results, the minimal set of bias voltages is $\{-3.0, -0.8, 1.0, 2.8\}$ volts, and the three weight vectors (one for each rock type) are $W1 = [15, -109, 32, 10]$, $W2 = [24, -63, -5, -8]$ and $W3 = [11, 3, -128, 24]$ [5]. Figure 2 illustrates a schematic of the rock-type separation based on the algorithm discussed above.

The hardware implementation of this algorithm requires a processing unit to multiply each photocurrent by each one of the weights. Unfortunately, this unit will require an extended area of the unitcell, making it impossible to implement in practice. Therefore, in [5] a further refinement of the algorithm was proposed which embeds the multiplication (by weights) and addition in the photocurrent integration process by appropriately adjusting the bias scheme of the DWELL continuously in time. In this paper we discuss the hardware design and implementation of the continuous time-varying biasing approach reported in [5].

This paper is organized as follows. In Section II, the basic concept of the proposed spectrally tunable readout integrated circuit (ROIC) is discussed and the detail implementation of the algorithm in hardware is explained. In Section III, we discuss the test structure and the experimental results, and the conclusions are given in Section IV.

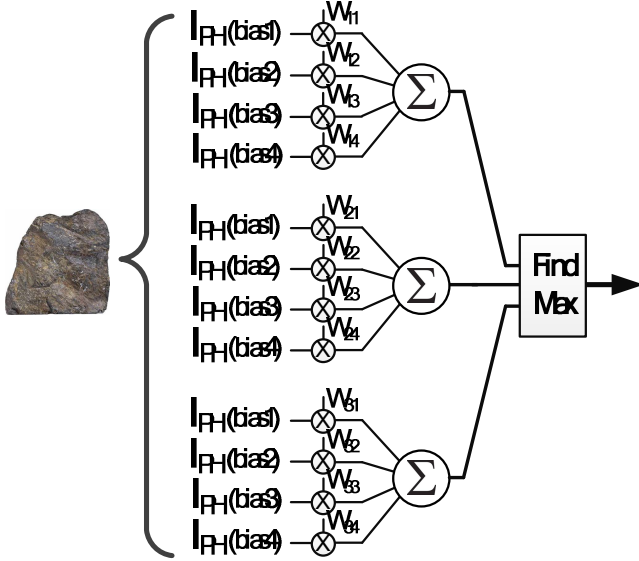


Fig. 2. Demonstration of the way weighted superposition algorithm [2] can be employed for multispectral classification

II. DESIGN ARCHITECTURE

Typically, a ROIC consists of a two-dimensional array of unitcells, where each of them is responsible for reading/integrating the photocurrent of one photodetector in the array. To access all pixels, a row and a column decoder addresses individual pixels and enables some switches to transfer the sampled data to a video amplifier at the output [6]. A detailed explanation of the implemented hardware is discussed below:

A. The unit cell

In order to benefit from high linearity and large dynamic range, we used a capacitive transimpedance amplifier (CTIA) configuration for the unitcell. A conventional CTIA unit cell is shown in Figure 3. As illustrated in the figure, the typical CTIA unitcell is composed of an integrator, a sample-and-hold (S&H) capacitor and a source-follower transistor to buffer the charge that is stored in the S&H capacitor. Two sets of analog multiplexers make the electrical connection between every pixel and the video amplifier.

To implement the multispectral classification discussed in the previous section, the circuit must be able to apply both positive and negative bias voltages to the photodetector [7]. The opamp with negative feedback in CTIA configuration ensures the polarity and value of the voltage on the negative input is the same as its positive input.

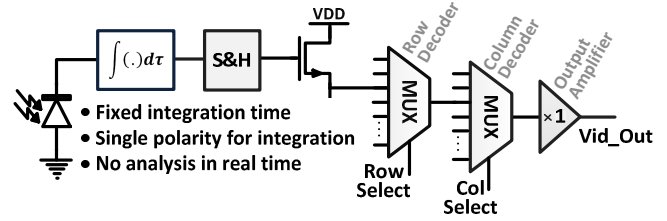


Fig. 3. Conventional CTIA unitcell and the multiplexers used to address different unitcells

Based on the weighted superposition algorithm reviewed earlier, the hardware required to implement multispectral classification must follow the procedure below:

- Apply proper bias voltage to the DWELL photodetector
- Integrate the photocurrent corresponding to the applied bias voltage for a specific time that is proportional to the first weight
- Apply second, third and fourth bias voltages to the DWELL photodetector and integrate the corresponding photocurrents over a time periods that are proportional to the associated weights
- Transfer the integrated photocurrent to the first S&H capacitor
- Repeat the procedure above for the second and third weight vectors and record the resultant charge in the second and third S&H capacitor.
- Compare the integrated voltage and recognize the rock type based on the relative magnitude of the voltages.

The implementation also requires multiplication of the photocurrent with both positive and negative weights. Therefore, the hardware must have the ability of integration in both polarities of the photocurrent. Figure 4.a shows a revised CTIA that performs the required tasks listed above. The four switches in Figure 4.b control the polarity of integration. When the switches labeled 1 are connected, the photocurrent charges/discharges the capacitor and when the switches labeled 2 are connected the polarity of integration is reversed. To reset the integration capacitor all the four switches must be connected.

As discussed earlier, applying the three sets of weight vectors to the photocurrents while the photodetector is biased properly will result in three different voltages that must be mutually compared to produce the rock type that is being imaged by the sensor. Figure 4.c shows the three S&H capacitors needed to store the superimposed value. As shown in the figure, the three capacitors are controlled using three separate S&H switches. The output of these three capacitors is connected to a block to compare their relative value and produce the type of rock.

To implement the block diagram above in silicon, there would be a need to implement about 35 transistors and five capacitors (one compensation capacitor for the opamp, one integration capacitor and three S&H capacitors). Because of the large number of transistors and capacitors, this block

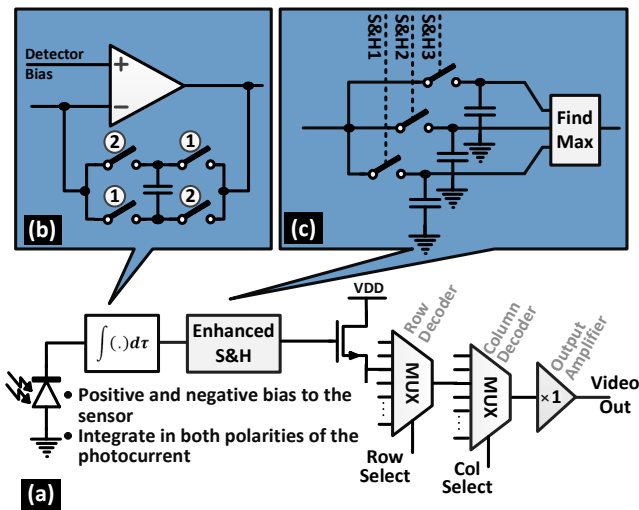


Fig. 4. a) A CTIA unitcell capable of multispectral classification b) configuration of the integration capacitor and the four switches to control the integration polarity c) three S&H capacitor and the analog comparison block

diagram is not suitable for unitcell designs. Instead, a revised version of the block diagram is proposed and shown in Figure 5, where it utilizes less area than that shown in Figure 4 and performs equally well. The revised unitcell has only one compensation capacitor, a S&H capacitor and an integration capacitor that also work for the S&H purpose.

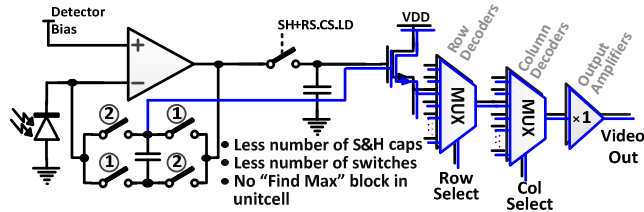


Fig. 5. Revised block diagram of the unitcell proposed for multispectral classification

In the revised block diagram, the first integrated sample, corresponding to the first weighted superposition, is transferred to the S&H capacitor. The second and third samples, while the integrated sample is in the integration capacitor, are compared against what is stored in the S&H capacitor and transferred to the S&H capacitor only if it is larger than the S&H value. If the comparator that is located outside the unitcell decides, where the new value stored in the integrator capacitor, is not larger than the old value stored in the S&H capacitor, the integrated value will be discarded. The proposed design also has the extra benefit that the number of weighted superposition is not restricted to three. As the hardware keeps only the largest and the recent sample, it is practically capable of performing any number of comparisons. Figure 6 demonstrate the proposed unitcell and analog switches for the output video signal in switch level. Since the opamp output voltage is a function of the photocurrent that is injected to integration capacitor and the sampling time is not the same for all the pixels, in Figure 6 the

output is taken from different node. The block diagram of the proposed readout integrated circuit is shown in Figure 7.

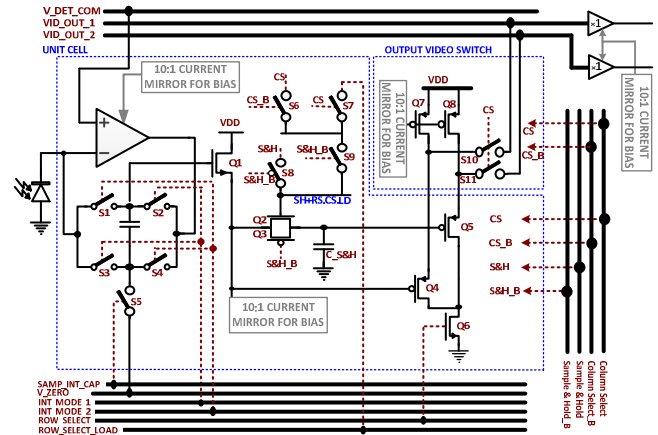


Fig. 6. Switch level demonstration of the proposed unitcell and the switches for the video signal

B. IC fabrication

The algorithm imposes the requirement to apply bias voltage in the range -5 to +5 volts to the DWELL photodetector. Therefore, the readout circuit must be able to provide a minimum dynamic range of 10 volts. We have designed and fabricated the chip based on the standard 0.35 μm mixed-signal 3.3V/15V TSMC High Voltage CMOS process. The process supports for two poly and four metal layers. To benefit from the high dynamic range at the input and output, most parts of the chip are designed using high voltage transistors.

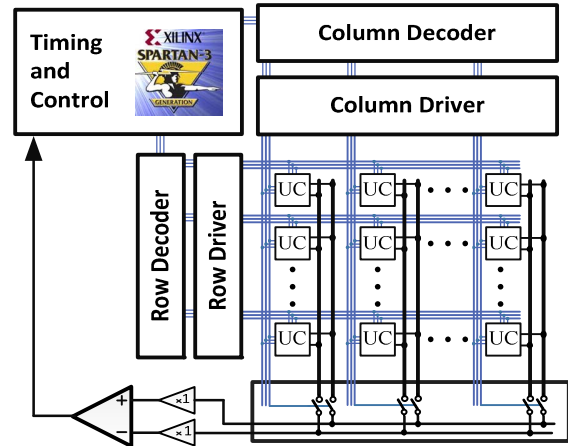


Fig. 7. Block diagram of the proposed readout circuit for multispectral classification

III. EXPERIMENTAL RESULTS

A microphotograph of the chip is shown in Figure 8.a. The total dimension of die is 6052 μm by 5452 μm . Simulation, design and post-layout verification for the readout circuit, amplifiers and ESD protection were performed entirely in Tanner EDA tools; however, as TSMC does not provide the setup file for layout and the extraction command file for L-Edit, these file was also built by our group. For extra

verification, the final design was imported to Cadence Virtuoso to verify all the DRC rules. A picture of the unitcell that is designed in L-Edit is shown in Figure 8.b.

A Xilinx MicroBlaze Development Spartan-3E 1600E board is used to generate control signals and a PCB board was designed to enhance signal integrity. A picture of the PCB board connected to the Xilinx FPGA board is shown in Figure 8.c.

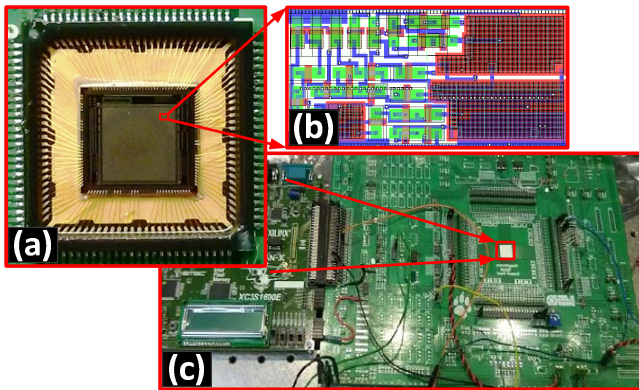


Fig. 8. The test setup a) A microphotograph of the chip b) a picture of the unitcell designed in L-Edit c) a picture of the PCB board designed to test the chip and the Xilinx FPGA board that generates the control signals.

The dimension of each pixel in the designed readout circuit is $30\ \mu\text{m}$ by $60\ \mu\text{m}$. The reason of having a non-symmetric dimension for the unitcell is to have a consistent pitch with the focal-plane arrays (FPAs) and also have enough room to fit the large number of transistors and capacitors needed to implement the classification algorithm. The readout circuit designed for multispectral classification was successfully tested. Figure 9 shows a picture of the video signal and also the row-select/column select pulses that are serially shifted out after selecting all the rows/columns. The shown results demonstrate that the designed ESD protection, row/column decoders, row/column drivers, video signal buffers and the unitcell are entirely functional for the desired application. Moreover, based on the test points that we laid out in the design, the video signal generated in the test chip is also verified. Our next step is to hybridize the DWELL FPA to the readout circuit, followed by the test of the chip in real-time rock classification. Table I summarizes some specifications of the chip.

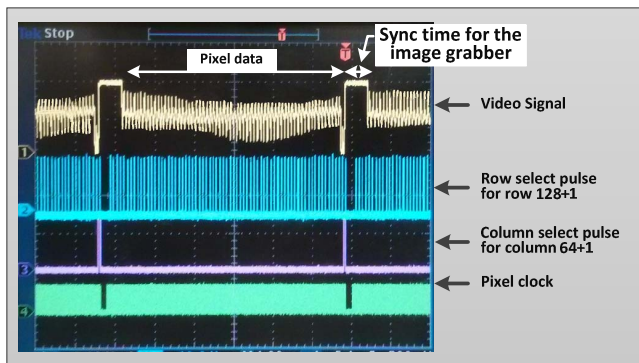


Fig. 9. The video signal and the row/column pulse that shifts out of the last row/column

TABLE I. SPESEIFICATIONS OF THE READOUT INTEGRATED CIRCUIT DESIGNED FOR MULTISPECTRAL CLASSIFICATION

Transistor # in unitcell	26	Technology	TSMC 0.35 μm HV
Capacitor # in unitcell	3	Photodetectors	DWELL
Integration capacitor	199 fF	Input sig. swing	13.0 V
S&H capacitor	228 fF	Output sig. swing	12.5 V
Compensation capacitor	34 fF	Power supply	15/3.3 V
Transistors bias current	1 μA	Unit cell dimension	30 x 60 μm^2
Unitcell array Size	128x64	Chip dimension	6052 μm x 5452 μm

IV. CONCLUSIONS

In this paper, we discussed the design, outlined the fabrication, and presented the testing results of a single chip CMOS readout integrated circuit for multispectral rock classification. The input signals have a dynamic range of 13.0 volts in the input and 12.5 volts at output. The chip was fabricated through MOSIS using TSMC's 0.35 μm HV CMOS technology. The designed readout circuit works with an array of 128x64 pixels, and is able to apply both positive and negative large bias voltages to the DWELL photodetector, change the integration polarity, and compare the integrated value against previously integrated sample to classify the rock type.

The test chip was successfully tested as an independent ROIC and it is now ready to be hybridized with a DWELL FPA. The proposed design is an ideal candidate for advanced smart-pixel imaging systems, such as real-time multispectral classification imaging, and infrared remote sensing imagers.

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