A Floating-Gate Trimmable High-Resolution DAC in Standard 0.25µm CMOS

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Abstract
We have built a 14-bit digital-to-analog converter (DAC) in a standard 0.25µm digital CMOS process. We use analog values stored on floating-gate p-channel MOSFETs to trim the DAC linearity. Because the storage is nonvolatile, we eliminate the need for continuous trimming. Our design has 6 untrimmable LSBs and 8 trimmable MSBs. The pre-trim differential and integral nonlinearity (DNL and INL) exceeded 140 and 200 LSBs, respectively; the post-trim DNL and INL are less than 2 LSBs. We were able to trim the 8 LSBs to 0.5 LSB linearity; the 2 LSB error is due to an untrimmable bit. Because our DAC does not require continuous trimming, nor laser-trimmable resistors, it occupies only 0.17 mm² of die area and dissipates 11 mW at 100 MHz with a –10 dBm differential output.

Introduction
Emerging standards for communications systems require digital-to-analog converters (DACs) with sample rates in the hundreds of MS/s, and resolutions of 10–14 bits [1]. System-on-a-chip integration poses additional constraints including low power dissipation, small die area, and compatibility with standard digital CMOS processing. Current-steering DACs are attractive for these applications because they are fast and can drive an output load without a voltage buffer. Their static linearity, however, is limited by process mismatch.

To reduce mismatch-induced DAC errors, designers may use large devices, randomized layouts, laser trimming, continuous online electrical trimming, or other special techniques [2-4]. These techniques always increase die area and power dissipation substantially. What DAC designers need is a small, nonvolatile, electrically trimmable current source. Our floating-gate pFETs [5] perform this function.

Floating-Gate pFETs
A floating gate pFET is a conventional p-channel MOSFET with no direct electrical connection to its gate. Because we use the pFETs as current sources, we have no need for a gate input. Consequently, we do not use a second poly layer in the design, ensuring compatibility with standard digital CMOS processing. We use Fowler–Nordheim (FN) tunneling [6] to remove electrons from the floating gate, and impact-ionized hot-electron injection (IHEI) [7] to add electrons to the floating gate. Hot-electron injection in a pFET is a very precise and controllable process, so we can store accurate analog values on the floating gate [8]. We show a floating-gate pFET in Fig. 1.

The DAC
Fig. 2 shows a DAC block diagram. We use a segmented architecture with 6 binary-decoded lower LSBS (LLSB), 4 binary-decoded upper LSBS (ULSB) and 4 thermometer-decoded MSBs. The on-chip calibration circuitry trims the ULSB and MSB segments, while the LLSB segment relies solely on intrinsic matching. The digital circuitry comprises a static register to latch the 14-bit input word. The lower 10 flip-flops drive binary-weighted current-source arrays (6 LLSB and 4 ULSB), while the upper 4 bits are thermometer decoded to drive 15 identical current sources.

Nineteen trim pFETs allow us to increase the outputs of the 4 ULSB and 15 thermometer-decoded MSB current sources. A pFET’s current is unipolar, so the trim transistors by themselves do not provide bidirectional trimming. We add floating-gate pFET based current-regulation circuits to trim the current reference for each segment, allowing bidirectional trimming.

We trim the DAC using the following procedure: We first erase all the trim transistors by applying a high voltage (~7V) to a global tunneling line. Then we trim each bit individually using electron injection, starting from the lowest ULSB. To trim ULSB bit i, we apply codeword 2i−1, add an extra LSB, and call the output current a target current. Next we apply codeword 2i, and trim bit i to cause the output current to match the target. To trim bit i+1 we apply codeword 2i+1−1, add the extra LSB, and trim bit i+1 to match the new target. To trim the thermometer-decoded current sources we use the same procedure, but incrementing the codeword in units of 1024 rather than by powers-of-two. We continue until we have adjusted all 19 trim pFETs.

We induce electron injection by applying a negative voltage (~2.5 V) to a trim pFET’s drain. We presently use off-chip supplies for the ~2.5 V injection and +7 V tunneling voltages, but will incorporate on-chip charge pumps in future designs. For the data in this paper we trimmed using lab instruments, but DACs presently in fabrication have an on-chip comparator and state machine for autonomous trimming. Fig. 3 shows the measured DNL and INL before and after trimming. The worst-case linearity of 2 LSBs is due to an untrimmable bit in the LSB segment, as well as reference-current noise. We trimmed all bits in the ULSB and MSB segments to 0.5 LSBs.

Our trim pFETs used 100 fF MOS capacitors for charge storage. We do not yet have data on long-term memory retention, but experiments running in the lab for 1 month show no evidence of charge loss to 14-bit accuracy at nominal temperature and supplies. Should charge loss become an issue for long (i.e. year) timescales, we can force the DAC to periodically self-trim during idle states or during power-up.

Fig. 4 shows a layout view of the DAC. The total active area is 0.17 mm²; the calibration circuitry occupies less than 10% of the area. The total power dissipation for a –10 dBm output is 11 mW at 100 MHz with a 3.3 V power supply.

Conclusion
We have described a CMOS DAC that uses floating-gate pFETs for electrical trimming. Because we trim the current-source transistors themselves, the power and area are significantly less than existing high-linearity DACs. Furthermore, we can fabricate our DAC in any standard CMOS process in which we can build low-leakage floating-gate pFETs.
A. Top View

B. Side View

Figure 1. A floating-gate pFET and its associated tunneling junction, showing the electron tunneling and injection locations.

Figure 2. DAC block diagram. A digital register latches the input word, where the 4 MSBs are thermometer-decoded. LLSB is an untrimmable current source array, while ULSB and MSB are trimmable current-source arrays. The output is a differential current. The injection and tunneling lines control trimming.

Figure 3. (a) DNL and (b) INL before trimming; (c) DNL and (d) INL after trimming. We were able to trim the ULSBs and MSBs to a DNL and INL of 0.5 LSBs; the points between 0.5 and 2 LSBs are due to an untrimmable bit.

Figure 4. Layout view. The total active area is 0.17 mm², the current-source arrays occupy 0.10 mm², the trimming section occupies 0.02 mm², and the digital circuits use 0.02 mm².

References