Currículum Vitae
Miguel Figueroa

Información de Contacto

- Email: miguel.figueroa < A T > udec.cl
- Teléfono: +56(41)220-4776
- Fax: +56(41)224-6999
- Dirección Postal

  Departamento de Ingeniería Eléctrica
  Universidad de Concepción
  Casilla 160-C
  Concepción
  Chile

Grados Académicos

- Ph.D. (Computer Science & Engineering), University of Washington, USA, 2005.
- M. Sc. (Computer Science & Engineering), University of Washington, USA, 1999
- M. Sc. (Ingeniería Eléctrica) Universidad de Concepción, Chile, 1997
- Ingeniero Civil Electrónico, Universidad de Concepción, Chile, 1991
- Licenciado en Ciencias de la Ingeniería Electrónica, Universidad de Concepción, Chile, 1988

Experiencia Académica

- Profesor Asociado, Departamento de Ingeniería Eléctrica, Universidad de Concepción, 2005 – a la fecha.
- Profesor Asistente, Departamento de Ingeniería Eléctrica, Universidad de Concepción, 1994 – 2005 (con permiso durante 1997 – 2003).
- Ayudante de Investigación, Department of Computer Science & Engineering, University of Washington, 1999-2003.
- Ayudante de Docencia, Department of Computer Science & Engineering, University of Washington, 1997-1998.
- Lecturer, Departamento de Ingeniería Eléctrica, Universidad de Concepción, 1992.
- Lecturer, Departamento de Ingeniería Informática y Ciencia de Computación, Universidad de Concepción, 1991.

Experiencia Profesional

- Consultor, calibración de circuitos análogos en chip y tecnología de compuerta flotante, Impinj, Inc. (USA), 2001-2002.
- Consultor para varias empresas chilenas en software de tiempo real y redes (Chile), 1994-1997.
- Ingeniero de Software, Sonda Sistemas de Automatización, Ltda. (Chile), 1993-1994

Premios y Becas

- Beca Presidente de la República para estudios de postgrado en Universidades extranjeras, MIDEPLAN, Chile, 1997-2000
- Beca Fullbright/LASPAU para estudios de postgrado en Universidades norteamericanas, 1997-1999.
- Beca CONICYT para estudios de Magister en Universidades chilenas, CONICYT, Chile, 1991-1992.
- Premio Universidad de Concepción al major estudiante de la carrera de Ingeniería Civil Electrónica, 1991.

Proyectos de Investigación

- Proyecto Fondecyt No. 1040617, “Correlational Learning Algorithms in Analog and Mixed-Mode CMOS,” 2004 - 2006.

Patentes

- A Method and Apparatus for Trimming a Digital to Analog Converter (US Patent 6,664,909). Estado: Concedida, EE. UU..
- Variable Delay Circuits (US Patent Application No. 10/666,789). Estado: En proceso, EE. UU.

Publicaciones

Publicaciones en Revistas

1. Gonzalo Carvajal, **Miguel Figueroa** and Seth Bridges, “Effects of Analog-VLSI Hardware on the Performance of the LMS Algorithm,” *Springer-Verlag Lecture Notes in Computer Science*, No. 4131, pp. 963-973, September 2006.
2. **Miguel Figueroa**, Seth Bridges and Chris Diorio, “A 19.2 GOPS Mixed-Signal Filter with Floating-Gate Adaptation”, *IEEE Journal of Solid State Circuits*, Vol. 39 No. 7, pp. 1196-1201, July 2004.
3. John Hyde, Todd Humes, Chris Diorio, Mike Thomas and **Miguel Figueroa**, “A 300 MS/s, 14-bit, Digital-to-Analog Converter in Logic CMOS”, *IEEE Journal of Solid State Circuits*, Vol. 38 No. 5, pp. 734-740, May 2003.
4. David Hsu, **Miguel Figueroa** and Chris Diorio, “Competitive Learning with Floating-Gate Circuits”, *IEEE Transactions on Neural Networks*, Vol. 13, No. 3, pp. 732-744, May 2002.
5. Chris Diorio, David Hsu and **Miguel Figueroa**, “Adaptive CMOS: From Biological Inspiration to Systems on a Chip”, *Proceedings of the IEEE*, Vol. 90, No. 3, pp. 345-357, March 2002.
6. **Miguel Figueroa**, David Hsu and Chris Diorio, "A Mixed-Signal Approach to High-Performance, Low-Power Linear Filters," *IEEE Journal of Solid State Circuits*, pp. 816-822, Vol. 36 No. 5, May 2001.
7. **M. E. Figueroa**, L. A. Lagos y E. Young. “A Client/Server Platform for Distributed Access to SCAUT-3G Resources (in Spanish),” *Revista de Automática e Innovación*, pp. 49-56, No. 7, Vol. 2, 1995.
8. J. H. Moreno, R. Sánchez, L. A. Lagos y **M. E. Figueroa**. "Introducing CAD/CAE Tools in Digital Systems Education (in Spanish)," *Informativo de Electricidad*. May-June, 1992.
9. J. H. Moreno, **M. E. Figueroa** and T. Lang. "Linear Pseudosystolic Array for Matrix Algorithms". *Journal of VLSI Signal Processing*; 3, 201-214 (1991). Kluwer Academic Publishers.

Publicaciones en Conferencias

10. Seth Bridges, Jeremy Holleman, Ania Mitros, Chris Diorio and **Miguel Figueroa**, “A Random-Projection Imager for Visual Pattern Classification in Analog VLSI,” in *Proceedings of the 2006 European Conference on Solid-State Circuits (ESSCIRC)*, pp. 428-431, Montreux, Switzerland, September 18-22, 2006.
11. Gonzalo Carvajal, **Miguel Figueroa** and Seth Bridges, “Effects of Analog-VLSI Hardware on the Performance of the LMS Algorithm,” in *Proceedings of the 2006 International Conference on Neural Networks (ICANN)*, published by Springer-Verlag Lecture Notes in Computer Science, No. 4131, pp. 963-973, Athens, Greece, September 10-14, 2006.
12. **Miguel Figueroa**, Esteban Matamala, Gonzalo Carvajal and Seth Bridges, “Adaptive Signal-Processing in Mixed-Signal VLSI with Anti-Hebbian

Learning", in Proceedings of the *2006 IEEE Computer Society Annual Symposium on VLSI*, pp. 133-138, Karslruhe, Germany, March 2-3, 2006.

13. Seth Bridges, **Miguel Figueroa**, David Hsu and Chris Diorio, "A Reconfigurable VLSI Learning Array", in *2005 IEEE European Solid-States Circuits Conference*, pp. 117-120, Grenoble, France, September 12-15, 2005.
14. **Miguel Figueroa**, Seth Bridges, and Chris Diorio, "On-Chip Compensation of Device-Mismatch Effects in Analog VLSI Neural Networks", in *Advances in Neural Information Processing Systems*, pp. 441-448, Vancouver, BC, Canada, December 14-16, 2004.
15. **Miguel Figueroa**, Seth Bridges, David Hsu and Chris Diorio, "A 19.2GOPS, 20mW Adaptive FIR Filter", in *2003 IEEE European Solid-States Circuits Conference*, pp. 509-512, Estoril, Portugal, September 16-18, 2003.
16. David Hsu, Seth Bridges, **Miguel Figueroa** and Chris Diorio, "Adaptive Quantization and Density Estimation in Silicon", in *Advances in Neural Information Processing Systems*, pp. 1083-1090, Vancouver, BC, Canada, December 9-14, 2002.
17. Seth Bridges, **Miguel Figueroa**, David Hsu and Chris Diorio, "Field-Programmable Learning Arrays", in *Advances in Neural Information Processing Systems*, pp. 1155-1162, Vancouver, BC, Canada, December 9-14, 2002.
18. John Hyde, Todd Humes, Chris Diorio, Mike Thomas and **Miguel Figueroa**, "A Floating-Gate Trimmed, 14-bit, 250 MS/s Digital-to-Analog Converter in Standard 0.25μm CMOS", in *2002 IEEE Symposium on VLSI Circuits*, Digest of Technical Papers, pp 328-331, Honolulu, Hawaii, USA, June 14-16, 2002.
19. **Miguel Figueroa**, John Hyde, Todd Humes and Chris Diorio, "A Floating-Gate Trimmable High-Resolution DAC in Standard 0.25μm CMOS", in *2001 IEEE Non-Volatile Semiconductor Memory Workshop*, pp. 46-47, Monterey, CA, USA, August 12-16, 2001.
20. David Hsu, **Miguel Figueroa**, Chris Diorio, "A silicon primitive for competitive learning," in *Advances in Neural Information Processing Systems*, pp. 1087-1096, Denver, Colorado, December 12-16, 2000.
21. **Miguel Figueroa** and Chris Diorio, "A 200MHz, 3mW, 16-Tap Mixed-Signal FIR Filter," in *2000 Symposium on VLSI Circuits*, Digest of Technical Papers, pp 214-215, Honolulu, Hawaii, June 15-17, 2000.
22. Tim Tuan, **Miguel Figueroa**, Frank Lind, Chucai Zhou, Chris Diorio, John Sahr. "An FPGA-Based Array Processor for an Ionospheric-Imaging Radar," in *Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 313-314. Napa Valley, California. April 17-19, 2000.
23. Darren C. Cronquist, Chris Fisher, **Miguel Figueroa**, Paul Franklin and Carl Ebeling, "Architecture Design of Reconfigurable Pipelined Datapaths," in *Proceedings of the 20th Anniversary Conference on Advanced Research in VLSI*, pp. 23-40. Atlanta, Georgia, USA, March 21-24, 1999.
24. **M. E. Figueroa** and J. F. Otth, "A System for Distributed Management of TCP/IP Networks (in Spanish)," in *XII Conferencia de la Asociación Chilena de Control Automático*, pp. 249-256, Santiago, Chile, November 18-22, 1996.

25. S. Jaque and **M. E. Figueroa**, “Performance Evaluation of an Ethernet Network Using a TCP/IP Stack (in Spanish),” in *XI Congreso Chileno de Ingeniería Eléctrica*. Punta Arenas, Chile. November 13-17, 1995.
26. R. Sánchez, **M. E. Figueroa**, E. Jansson and L. Longeri, “A Supervisory System for a Bottling Line,” in *XI Congreso Chileno de Ingeniería Eléctrica*. Punta Arenas, Chile. November 13-17, 1995.
27. **M. E. Figueroa**, “An Enhanced Programmable Pseudosystolic Processor for Matrix Algorithms,” in *Proceedings of the XV International Conference of the Chilean Computer Science Society*, pp. 222-231, Arica, Chile. November 1-3, 1995.
28. **M. E. Figueroa**, L. A. Lagos and E. Young, “A Client/Server Platform for Distributed Access to SCAUT-3G Resources (in Spanish),” in *XI Conferencia de la Asociación Chilena de Control Automático*. Concepción, Chile. November 7-11, 1994.
29. **M. E. Figueroa** and E. Young, “A Programmable Operator’s Interface for a Global Plant Automation System (in Spanish),” in *XI Conferencia de la Asociación Chilena de Control Automático*. Concepción, Chile. November 7-11, 1994.
30. **M. E. Figueroa** and J. H. Moreno, “Mapping Matrix Algorithms onto a SIMD Array Processor,” in *Proceedings of the XII International Conference of the Chilean Computer Science Society*, pp. 235-248, Santiago, Chile. October 14-16, 1992.
31. **M. E. Figueroa** and J. H. Moreno, “Modeling and Simulation of a Pseudosystolic Processor for Matrix Algorithms,” in *Proceedings of the XI International Conference of the Chilean Computer Science Society*, pp. 419-432, Santiago, Chile, October 15-18, 1991, Also in "*Computer Science. Research and Applications*," pp. 419-430, Plenum Press, 1992
32. J. H. Moreno and **M. E. Figueroa**, “A Decoupled Access/Execute Processor for Matrix Algorithms: Architecture and Programming,” in *Proceedings of the 1991 International Conference on Application-Specific Array Processors*, pp. 281-295, Barcelona, Spain, September 2-4, 1991.
33. J. H. Moreno and **M. E. Figueroa**, “A Linear Array for Matrix Algorithms (in Spanish),” in *IX Conferencia de la Asociación Chilena de Control Automático*, pp. 389-394, Pucón, Chile, October 29 - November 2, 1990.